

**Amendments to the Specification:**

Please replace paragraph 8 with the following amended paragraph:

**[0008]** Fig. 3 shows a system according to embodiments; and

Please replace paragraph 17 with the following amended paragraph:

**[0017]** Fig. 3 shows components of a system according to embodiments of the invention. In Fig. 3, a cache 102 contains at least one cache line 300. The cache line 300 corresponds to data, for example, program instructions, application or user data, and internal flags and state data, associated with operations being performed by a processor. As part of the operation of fetching data from the cache line, a calculated parity 301 and an expected parity 302 for the cache line may be generated. The expected parity may be generated, for example, when data loaded into the cache is retrieved from a less proximate memory such as an L2 cache or from main memory 100 (see Fig. 1) via an external bus. The calculated parity may be calculated when the data is read out of the cache 102.

Please replace paragraph 24 with the following amended paragraph:

**[0024]** As shown in block 502, the soft error handler may then retrieve recovery information from the soft error recovery memory. For example, this information could be the address or index, saved earlier, of the cache line 300 (see Fig. 3) being fetched, in which a soft error was detected. Then, as shown in block 503, the soft error handler may perform a cache clearing operation at one of multiple possible levels. For example, the cache in its entirety may be flushed.

Alternatively, only the cache line in which the soft error was detected may be cleared, using the cache line address obtained from the soft error recovery memory. More specifically, the cache line may be "invalidated", which is an operation which on a subsequent fetch to the same address will cause a cache miss to be registered and consequently, the corresponding cache line to be reloaded from external memory. Alternatively, an intermediate portion of the cache, i.e., a range of cache address space between the full cache and a single cache line, but including the cache line in which the soft error has been detected, may be cleared.